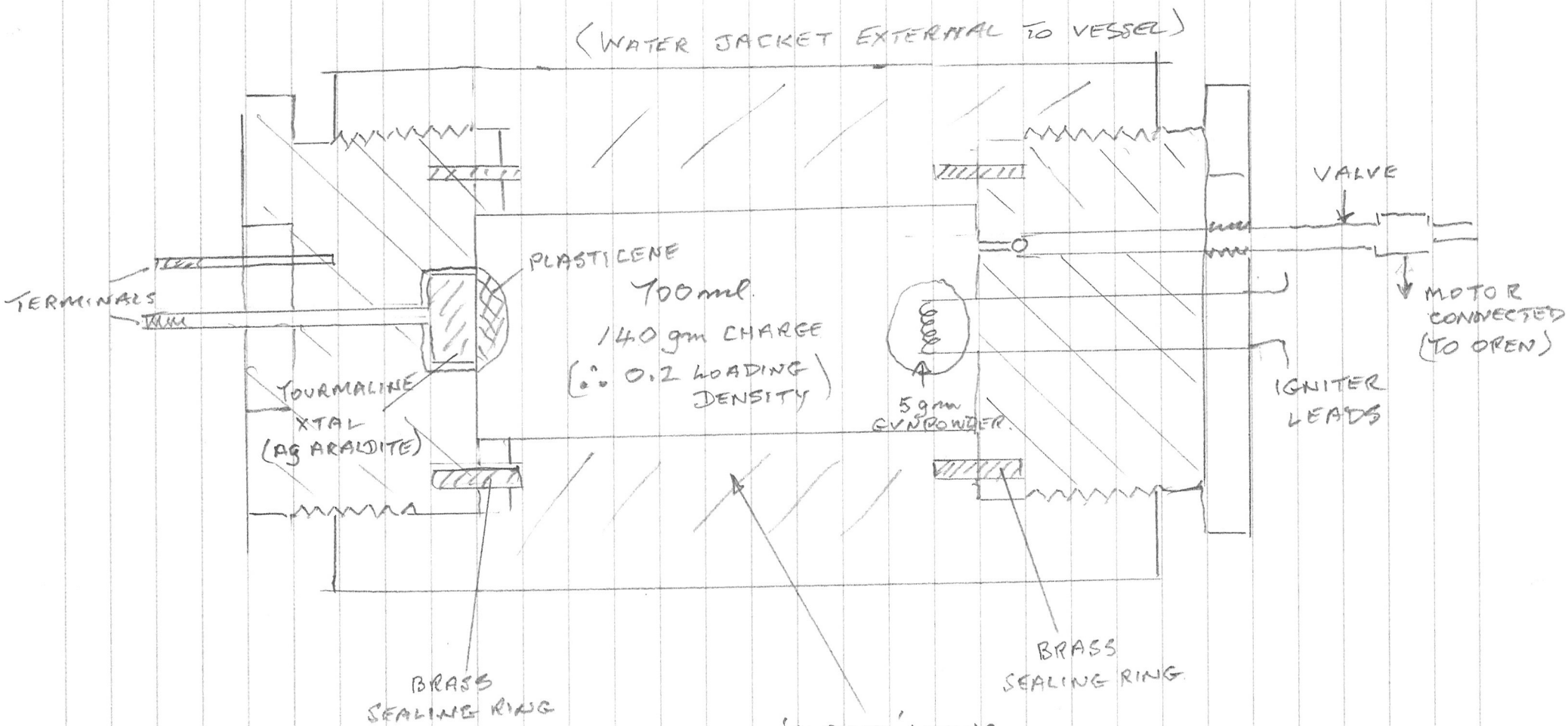
WASC 1855

Apparatus Report
Circuit Design
for
Closed Vessel
Signal Simulator

D. Eldridge

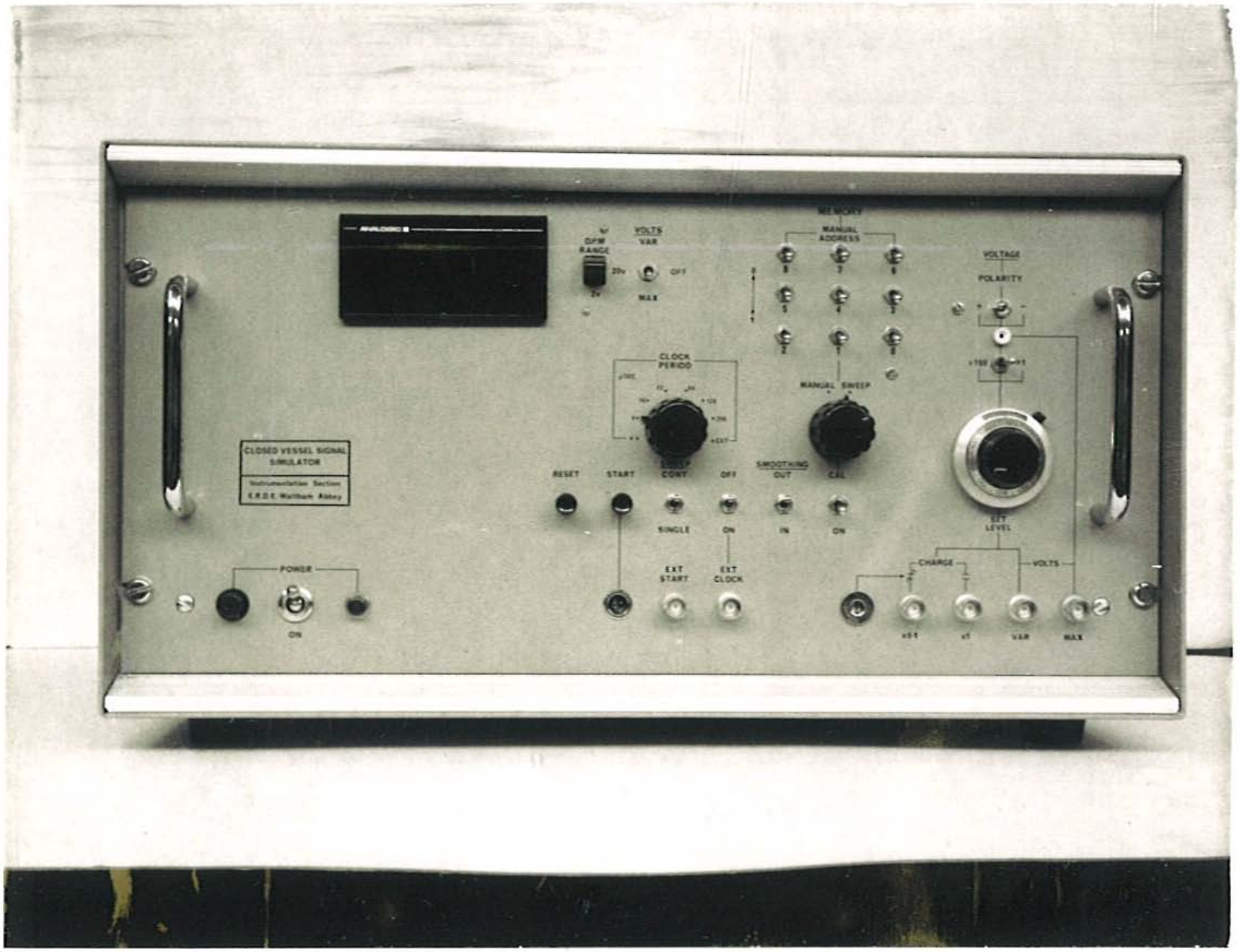
300 MPa (20 T.S.I.) LARGE CLOSED VESSEL



SKETCH FROM MEMORY

B. C. HOWARD

JAN 2011



CLOSED VESSEL SIGNAL SIMULATOR

E.R.D.E.

WALTHAM ABBEY

ELECTRONICS SECTION

APPARATUS REPORT

CIRCUIT DESIGN FOR CLOSED VESSEL SIGNAL SIMULATOR

DATE
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AR 239

CIRCUIT DESIGN FOR CLOSED VESSEL SIGNAL SIMULATOR

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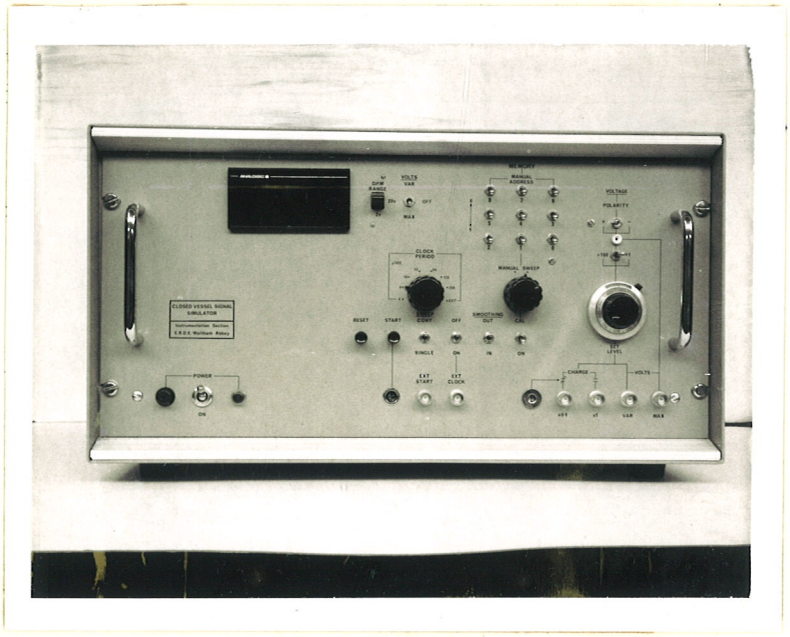
Instrumentation Section
ERDE



CLOSED VESSEL SIGNAL SIMULATOR

CIRCUIT DESIGN FOR CLOSED VESSEL SIGNAL SIMULATOR

Figs

CIRCUIT DESIGN FOR CLOSED VESSEL SIGNAL SIMULATOR AR 239

Introduction

Until a few years ago all Closed Vessel work whether in research and development, production or inspection areas was carried out using the standard "Cintel" recorder. Since this time a number of new equipments have been purchased, these being mostly computerised and not standard with each other. This has led to some discrepancy in results and apart from using standard propellant charges there is no way of cross checking between equipments. Also, since charge weight, vessel temperature and volume etc must be taken into consideration when evaluating results then there is no way of isolating the performance of the recorder from the vessel transducer combination.

The requirement for a standard Closed Vessel Signal Simulator was agreed at a CVR Working Party and the possible design approach was discussed in vague terms. No action was agreed other than that the problem would be looked at separately.

At ERDE some capacity became available for design development and construction and the possibility of developing a Simulator was discussed with the Ballistic Assessment Section who agreed to provide the necessary support for the work. No assistance was sought from other establishments but their possible requirements were borne in mind and appropriate facilities have been provided in the finalised prototype.

This report describes the design and development of the electronic circuits which are used to produce the required voltage waveforms. The design is based on considerations which are not discussed in this report but may be found in ERDE Apparatus Report No 238 "Calculations Relating to the Closed Vessel Simulator". It is important that this be read first to provide full understanding of the design philosophy for the electronic circuits.

Although the instrument has been designed for closed-vessel simulation other waveforms may be readily obtained (eg for rocketry simulation) simply by

changing the memories. Also, if required, repeated waveforms of appropriate shape can be obtained in "repeated sweep".

DESIGN CONSIDERATIONS

The requirement was for a waveform generator giving a voltage time or, for piezo electric transducer, charge-time characteristic similar to the pressure-time curve from a closed vessel firing. This is fully discussed in AR 238. The voltage output would be used for testing a system from the input point of an analogue-digital converter onward and the charge output would test a complete system including the charge amplifier.

A range of event times from 2.5 to 180 mSecs in seven steps was considered to be suitable for covering all requirements.

It was decided that, as far as possible the generated waveform should be traceable.

To cater for the inclusion of simulation of transducer calibration (where the output is reversed with respect to the operational polarity) and to allow for equipments which may operate with reverse polarity signals, both positive and negative outputs have been provided. A number of different "start" capabilities (manual, voltage pulse etc) and an adjustable "ignition delay" facility allow the instrument to be used as a direct replacement for a closed vessel ie it is indistinguishable from a closed vessel (plus transducer) as regards any recording system.

SYSTEM CONFIGURATION

A photograph of the completed instrument is shown at the front of this report. Fig 1 shows the system in block schematic form. Initiation is either by manual push button or by external voltage pulse or contact closure. Waveform generation starts when a gate opens after a delay (0.5 to 22.0 mSecs) allowing the 5MHz clock signal through the gate to a divide by ten counter giving a 500KHz clock signal. This then feeds a chain of binary dividers

giving voltage pulses having periods of 4, 8, 16, 32, 64, 128 or 256 μsecs and these are the effective clock pulses for the system. These clock pulses feed a binary counter and this, if switched to "Sweep", is used to address the Programmable Memory Stack. This stack is in effect a large Read Only Memory thus as it is addressed by the binary counter, the address incrementing from 0 to 511 at the clock rate. On reaching "511" a circuit is used to operate a stop circuit which closes the gate through which the original 5 MHz signal is entering the system. The time taken to sweep through to the 511 condition is 510 times the clock period giving, for the available clock rates, total event times of 2.04, 4.08, 8.16, 16.32, 32.64, 65.28 and 130.56 mSecs. It should be noted however that as will be mentioned later filtering action can extend these times to approximately 2.5, 5, 10, 20, 40, 80 and 160 mSecs.

The Read Only Memory outputs a 12 bit binary number and this, fed to the Digital-Analogue Converter, produces a voltage. The memory is programmed such that the output when converted produces a voltage at each address which is in accordance with the required characteristic for simulating the Closed-Vessel waveform. This is discussed fully in AR 238.

An inverting amplifier provides a negative signal. The required polarity is selected and the signal attenuated for feeding to a low impedance output voltage follower. Output from this can either be used direct providing a defined waveform with a triangular dv/dt/V characteristic or by feeding through an appropriately valued capacitor we obtain charge output similar to that obtained from the piezo-electric transducer on the closed-vessel.

The output signal may be smoothed if required. The full implications of smoothing are again discussed in AR 238.

A digital panel meter is provided to assist in monitoring and this is very useful for checking the output at a particular address when the memory is switched to Manual and addressing is done by the Manual Address Switches. The "Cal" switch can be used to cause the Memory/DAC combination to give zero or a set level of output which may be equated to a particular pressure level in the Closed Vessel. Thus a step pressure calibration may be obtained using this switch.

SPECIFICATION

Clock Interval	Overall Signal Duration Unsmoothed	Smoothed
4 secs	2.04 millisecs	2.8 millisecs
8 secs	4.07 millisecs	5.6 millisecs
16 secs	8.14 millisecs	11.2 millisecs
32 secs	16.29 millisecs	22.4 millisecs
64 secs	32.57 millisecs	44.8 millisecs
128 secs	65.15 millisecs	89.6 millisecs
256 secs	130.3 millisecs	179.2 millisecs
External	-	-

Signal Positive or negative

Output Voltage (max) 0-5.11V Ranges X1 and X.01

Output Charge 0-102, 200 pico-coulombs Ranges X1 and X.1

Start

Push Button
TTL Voltage Pulse
External contact closure

Ignition Delay

Adjusted internally 0.5-22 millisecs

Manual Address

The memory may be addressed by setting 9 switches to check memory output or to set a particular output voltage.

Mode

Reset Manual only

Single sweep or repeated sweep signals are available

DVM

Used to measure the output voltage 0-2V or 0-20V

CIRCUIT OPERATION

Gated Clock Pulse Generator - Fig 2 and Waveforms in Fig 11.

The functions of this circuit are:-

a) Cater for a range of start conditions.

b) Provide "Ignition Delay".

c) Provide a range of clock pulses.

d) Give a single or repeated sweep facility.

"Start" and "Ignition Delay"

All of the starting operations cause a positive voltage to appear on Pin 5 of the SN 74121N Monostable Multivibrator which triggers to produce a negative going pulse 0.5 to 22.0 mSecs duration at the output on Pin 1. Timing is set by R7.

The output from Pin 1 is applied to Pin 11 of the SN 7474 Edge Triggered Flip-Flop with triggering of this circuit occurring on the positive going portion of the input pulse ie after the delay period set on the monostable circuit. At the output (Pin 9 of the SN 7474) a positive voltage is obtained and this applied to the SN 7400N circuits opens both the "External Clock Pulses" gate, whose output (Pin 8) is routed through to the "Clock Period" switch (Ext) and also the gate which allows the crystal oscillator pulses (pin 3) through to the dividing circuits.

"Clock Pulses"

As was mentioned above external clocking may be obtained by applying suitable TTL compatible pulses to the "Ext Clock" socket and selecting on the "Ext Clock Period" switch. For other clock rates the output from the oscillator is taken through a gate to the input (Pin 1) of the SN 7400N counter which divides the 5 MHz oscillator signal by 10 providing a 500 KHz signal which is applied to a two SN 74293N binary divider chain giving frequencies of 250 Hz, 125 KHz etc for selection on the "Clock Period" switch.

"Single/Repeated Sweep"

This is simply effected by a switch which if required can give a "clear" signal to the SN 7474 circuit on Pin 13 on reaching the 511 condition (described elsewhere) thus providing single sweep by stopping the clock pulses or if left open then the sweep process continues with the counter continuing to deliver a repeated series of clock pulses at the output.

Waveforms appropriate to Card 1 are (1) to (7).

PROGRAMMABLE-MEMORY ADDRESS AND "STOP" SIGNAL GENERATOR - Fig 3 and Waveforms - Fig 11

This circuit board provides signals for addressing the memory incrementally. Other circuits detect when the address reaches a binary 511 ie 111111111 when an output signal reduces from a positive voltage to zero. It is this signal which may be selected to provide a "clear" signal to the SN 7474 unit on Card 1 to give "single sweep".

"Addressing"

Three SN 74161N four-bit binary counters are used for addressing the memory. These are synchronous so that all nine output memory addressing lines change simultaneously. Output count increments at the clock rate with the count stopping at 511 if operating on single sweep or reducing to zero with the next input pulse and starting again with continuous sweep.

"Single-Sweep"

The outputs from the counter are taken to a combination of gates comprising two 7420 Dual Four Input and one SN 7400 Quadruple Two Input Nand Gates. Three of the four-input gates are used on the counter output with following two-input gates used as inverters. The inverted outputs are taken to the remaining four-input gate with the result that when all counter outputs are high the final output (Stop Signal) goes low.

Waveforms applicable to Card 2 are (8) to (16).

PROGRAMMABLE-MEMORY STACK - Fig 4 - Fig 5

The requirement for memory is 511 12 bit words and this is achieved using three "512 x 4" devices. These are type 6305JA read-only memories manufactured by Memory Devices who also programmed them in accordance with requirements detailed in AR 238.

Fig 3 shows how the memories are addressed and outputted. The particular memories used require pull-up resistors in their outputs and as will be seen some of these are shunted with capacitors of various values. These capacitors are used to reduce the implitudes of "glitches" present in the output of the D-A converter and the value for the capacitors were obtained empirically.

The "cal" switch operates on the "enable" input to the memories. For the memories to operate, this input must be low otherwise all outputs are high regardless of the programmed code. In this "all high" condition the D-A converter gives out zero voltage thus the output can be made equal to zero or "calibration output" (as defined by memory address) according to the setting of the "cal" switch. Fig 5 shows how the memory may be addressed by the binary counter ("Sweep") or manually by a binary number where logic 1 corresponds to +5V.

ANALOGUE-DIGITAL CONVERTER - Fig 6

The converter - Analog Devices type DAC 12QZ BIN - is a complete component which plugs into the board shown on Fig 6. Gain and zero potentiometers are supplied with the board and by drilling through the board at points b, a and d the converter is programmed to give out approximately +10V when all inputs are high (approx 2.5 mV per bit). Gain is set to give out the appropriate voltage but it should be noted that this is not critical in relation to exact values since the signal suffers attenuation at a later stage (see Fig 8) whence a further control sets output at 1.25 mV per bit with max level for all inputs high of $4095 \times 1.25.10^{-3} = 5.12V$.

INVERTING AMPLIFIER - Fig 7

This is a normal negative-feedback amplifier. Unity-gain is achieved by using

components R_9, R_7 and R_3 with some slight effect due to the limiting resistor R11. Zero setting is obtained using R_1, R_2, R_4, R_5 and R_6.

The frequency response of the amplifier is not particularly good being approximately 3dB down at 110 KHz and an RC filter to give the same response is therefore provided for the output from the D-A card.

FILTERING, OUTPUT AND DIGITAL PANEL METER CIRCUITRY - Fig 8

The signal as selected from the "positive or negative" lines is attenuated to a level of 1.25 mV per bit which, for maximum signal output (4086 binary into D-A) gives 5.1075V. This signal may be further attenuated before application to the output amplifier using the " ÷ 100" switch (providing attenuation at constant impedance) or by adjustment of the "Set Level" control. This control is a plastic track low inductance potentiometer.

The implication of attenuation and also filtering which may be switched into the circuit are fully discussed in AR 238.

The particular output amplifier used was chosen because it provides unity gain to great accuracy with the ability to provide fairly high current into the output "charge" capacitor.

Monitoring of the output voltage is achieved using a $3\frac{1}{2}$ digit panel meter registering 1.999V full scale. The "20V" ranging is obtained using an attenuator with scale-adjust and also zero-adjust which is necessary to compensate for the effects of DPM input current. The decimal point moves in accordance with the setting of the range switch.

OUTPUT AMPLIFIER - Fig 9

This unity-gain amplifier provides both voltage and (through output capacitors) "charge" output. Decoupling capacitors on supply rails are fitted to reduce noise in the output to a minimum. Series resistance at the input is included to optimise the frequency-response characteristic. Zero adjustment is by means of R_4.

POWER SUPPLIES - Fig 10

These are stabilised. Connections are shown in Fig 10.

Current Consumption	+15V	35 mA
	-15V	40 mA
	+5V	600 mA

WAVEFORMS

These are present at points in the system which have already been noted above. They are all at TTL level and drawn ideally. In practice there are small steps in the "1" state with some of the waveforms. These steps are, however, of no consequence.

PERFORMANCE

The instrument has been designed to cover the following requirements:-

i) Checking of recorders to determine their accuracy as regards the measurement of pressure and rate of change of pressure with time.

ii) Determination of day to day changes in recorder performance.

iii) Cross-checking between equipments at various establishments.

iv) Generation of identical signals at a fast rate where, as in digital filtering for example, it is required to determine the effect on performance when changing the filter routine.

At ERDE checks have been made on the Honeywell computerised recording system. A filtering technique uses a number of samples centred around a particular measuring point to determine the "smoothed" value at that point. The number of samples may be selected within the software routine and it was required to determine the effects on the smoothed value with various numbers of samples. Fig 12 shows one result. The conditions chosen were as follows:

i) A smoothed generated waveform was used.

ii) "Maximum Pressure" was 15 T/sq in.

iii) "Action Pressure" was 9 T/sq in. This is beyond the point at which max dp/dt occurs - a condition not normally chosen but of no great consequence.

iv) The value of dp/dt for the simulated waveform was determined as shown in AR 238.

v) The value for dp/dt as evaluated by the recorder was plotted against group size (number of samples). Curve A relates to this experiment.

It will be seen that:

a) Increased group size gives lower values for dp/dt - a result which is not surprising but very informative.

b) The value for dp/dt at "zero" group size is the value which would be expected to be equal to the actual value (determined in (iv) above). This is not so.

A series of measurements at different simulated event times involving over thirty tests carried out in under three hours gave results which are expressed in Fig 13. This shows how the percentage error of the recorder evaluation increased with reducing event times. Although the errors were not severe considering the normal event times for CV firings it was apparent that there was a fundamental fault in the recording system. On investigation it was found that a differentiating amplifier in an oscilloscope, fed from the output of the charge amplifier, produced a very high capacitative shunting effect on the charge amplifier. This was corrected and the improvements in results are shown by curve B on Figs 12 and 13. There are obviously some small errors still to be investigated and these will be looked at in the future.

Conclusions

The instrument works well giving easily repeated waveforms thus eliminating the extremely tedious performance of setting up a closed vessel and firing it to obtain a single waveform.

The design has proved to be sound and performance up to the required standard. As with all prototypes however there are some improvements which cannot be incorporated in the existing instrument but should be considered for inclusion in future models. These are listed below.

Final proving of the instrument must be by a series of tests at ERDE followed by a comparison between ERDE and other establishments. Once these tests are complete any recommendations should be added to the list below.

Having proved the instrument the establishments concerned should decide whether or not to accept it as a piece of standard test equipment. In the event of this acceptance then the following points must be decided.

i) How many instruments are required?

ii) How is the funding to operate?

iii) How is the control of manufacture and testing to be carried out?

Suggested Improvements

1) As regards the memory the 512 x 12 bit arrangement is satisfactory but this does lead to an output with a fairly large initial step and the following steps being rather larger than desirable (1% of max) during the fast-rising portion of the output. Smoothing effectively eliminates this but obviously a "1024" memory arrangement would be an improvement and this could be limited to 10 bit without seriously degrading the system. The work involved in re-planning the memories should of course be taken into account regarding any change in design.

2) The D-A converter used in the prototype produces "glitches" ie large short duration negative going spikes superimposed on the output of the amplifier. The smoothed output is satisfactory but the unsmoothed (stepped) waveform from the D-A card is not good and it is for this reason that a certain degree of permanent filtering has been retained along with the slugging of some of the outputs from the memory. This trouble could be eliminated by using a strobed D-A converter where the strobe is implemented a short time (1.5μ secs

say) after clocking the synchronous counter which addresses the memory. This could be accomplished using a simple monostable delayed pulse generator.

3) The smoothing arrangement is not ideal since the capacitors used are large in value and not particularly stable. The arrangement shown in AR 238 is preferred. This would allow the use of a low value polystyrene capacitor which with non-inductive instrument type resistors would give better performance all round. Also the +10V signal and an inverted -10V signal could be used for application through a non-inductive potentiometer (or other non-inductive arrangement) to the circuit shown. This would lead to less work in using the tables in AR 238 and an added advantage would be that the charge capacitor at the output could be reduced to one half of the present value ie to 10,000 pF thus making it more like the piezo-electric transducer which is is simulating.

4) The smoothing resistors appropriate to the clock period could in a new arrangement be selected as now by using a separate wafer on the "Clock Period" switch. This wafer should be on a long shaft so that it is well removed from the digital switching thus reducing unwanted pick-up.

5) The power supply for output amplifiers should be situated close to these circuits. This would prevent supply lines running in cable forms along with digital lines which in the present model induces some noise into the output.

6) The DPM should have increased resolution eg 9.999V or 19.999V whence the complications of added circuitry and switching could be avoided. There is no reason why this meter should not be permanently in circuit.

OPERATING INSTRUCTIONS

Since it is not yet known how the instrument will be used it is not possible to lay down particular operating instructions but in any routine the following points must be considered.

i) The output signal starts at a nominal zero.

ii) The "start" operation increments the memory address.

iii) The memory steps through giving output voltages according to its programme, thus if it starts at an off zero voltage V_o then if the full voltage from the memory is V max the final output measured will be V_o + V max.

iv) The output at a particular address (dependent on smoothed or unsmoothed) is always the same fraction (K) of V max. This means that if the "Set Level" control is set to give say 0.15 V max then the output at the same address is now K. 0.15 V max. Thus it is important to keep this in mind when evaluating equivalent pressures or rates of change of pressure.

v) The instrument when simulating a transducer gives out charge. This may be equated to any pressure. Thus if we say that V max is equivalent to 15 T/sq in then in the example above the output at the address chosen (K = 0.6 say) would be equivalent to 9 T/sq in. If we had said that V max equated to 200 T/sq in then the output noted would equate to 120 T/sq in.

vi) Operating the "Cal" switch is equivalent to putting in a step of pressure. The amount of pressure depends upon what we have said V max is equal to eg in the above example we could have addressed the memory manually and operated the "Cal" switch thus putting in a step equivalent to 9 or 120 T/sq in dependent on what is equated to V max.

vii) Positive and negative signals may be obtained. It may be necessary to calibrate on one polarity and operate on the other. The DPM is useful in this respect for checking on the equivalence of the positive and negative signals.

viii) The repeated sweep facility is used only for maintenace and checking purposes.

SETTING-UP INSTRUCTIONS

i) Connect a sensitive digital voltmeter from the white test point on the front panel to earth. Press "Reset" then zero both the amplifier on the D-A card and the inverting amplifier using the appropriate controls.

ii) Press the "Start" button select positive and adjust the D-A amplifier

gain control to give a reading of 9.662V (whence the amplifier will be delivering 9.9771V at the top end of the 150 ohm resistor).

iii) Repeat zero and gain adjustments until both are correct.

iv) Select "negative" and repeat the above procedure using the zero and gain controls to again give a signal from 0 to -9.662V.

v) Connect the voltmeter now from the "Max V" output to earth. Adjust the "Scale" control (situated on the board attached to the front panel) to give a maximum voltage of 5.1075V (ie 4086 bits at 1.25 mV per bit).

vi) Connect the voltmeter to the VAR V output, turn the "Set Level" control to maximum and operate the reset button, the digital voltmeter should read zero. If not then reset zero using the zero control on the output amplifier underneath the chassis.

vii) Operate the start button. The digital voltmeter will then again read 5.1075V if the output amplifier is operating. DPM Check:- 2V Range.

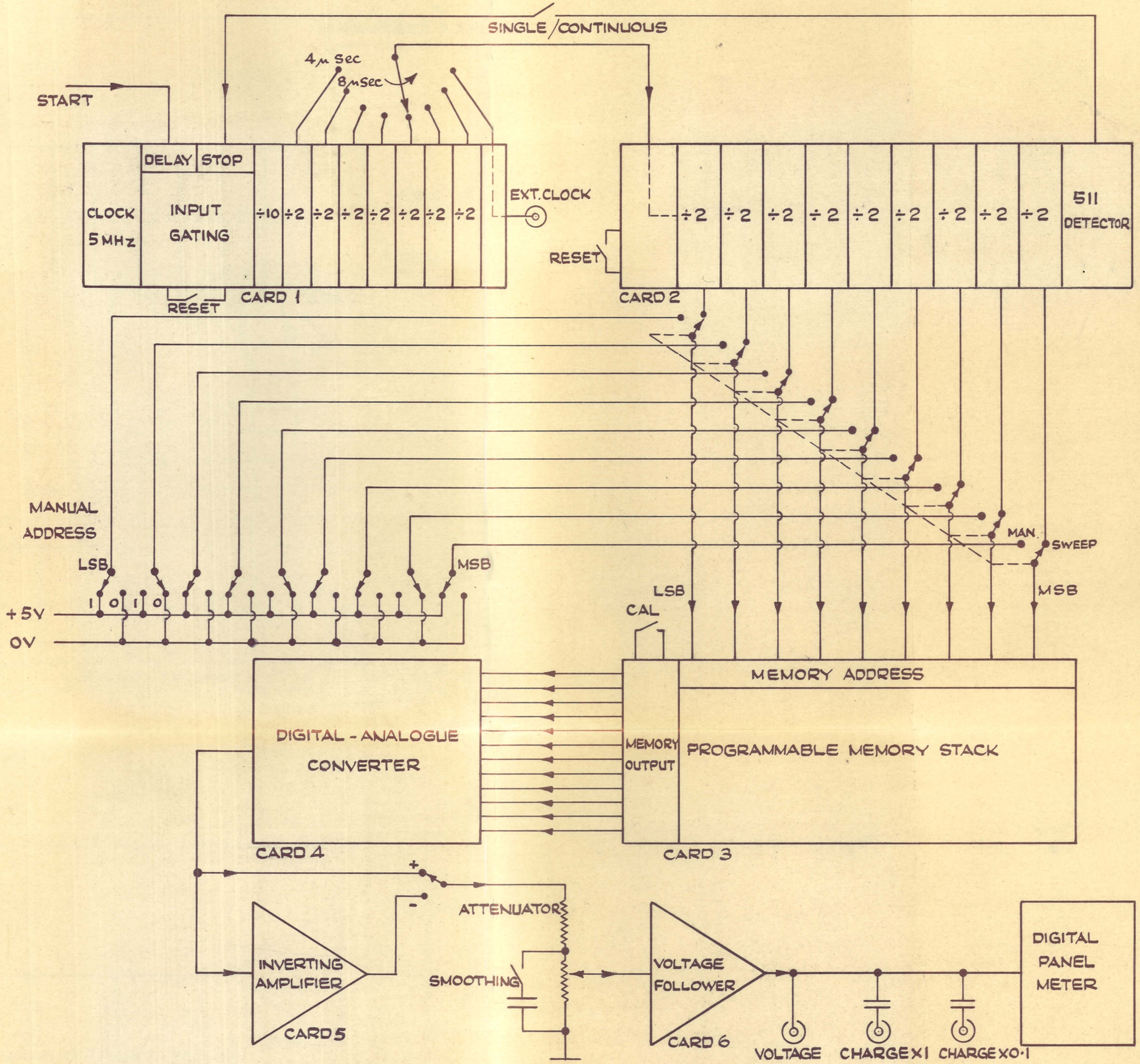
viii) Reduce the signal to about 1.4V using the Set Level Control. Operate the reset and select "2V" DPM range. The DPM should read zero - if not then reset it using its internal control.

ix) Operate the "Start" button. The DPM should read the same as the digital voltmeter. If not then adjust the DPM internal gain control. The procedure may need to be repeated adjusting first the zero and then the gain controls until correct.

DPM Check-20V range.

x) Turn the "Set Level" Control to maximum. Select "20V" DPM range and operate "Reset". The voltmeter should read zero. If not then adjust the "20V zero control" (identified by directional arrow on DPM).

xi) Operate "Start". The DPM should read 5.11. If not then adjust the 20V range control (again identified by arrow on DPM). It may be necessary to repeat zero setting followed by gain setting to finalise the adjustment.



AR 239 FIG 1 BLOCK SCHEMATIC OF SYSTEM DRG. Nº 1322

Key to Components

CARD 1 GATED CLOCK PULSE GENERATOR (Fig 2)

Integrated Circuits

74 Series		Texas Insts

Resistors

1	1K5	MR5	Welwyn
2	1K5	MR5	Welwyn
3	270R	MR5	Welwyn
4	270R	MR5	Welwyn
5	1K5	MR5	Welwyn
6	330R	MR5	Welwyn
7	20K	Flatpot	RS Components
8	330R	MR5	Welwyn

Capacitors

1	0.1 μF	250V	RS Components
2	0.01 μF	Ceramic 831	Erie
3	0.01 μF	PMA	ITT
4	0.01 μF	Ceramic	Erie
5	1.5 μF	PMC	ITT

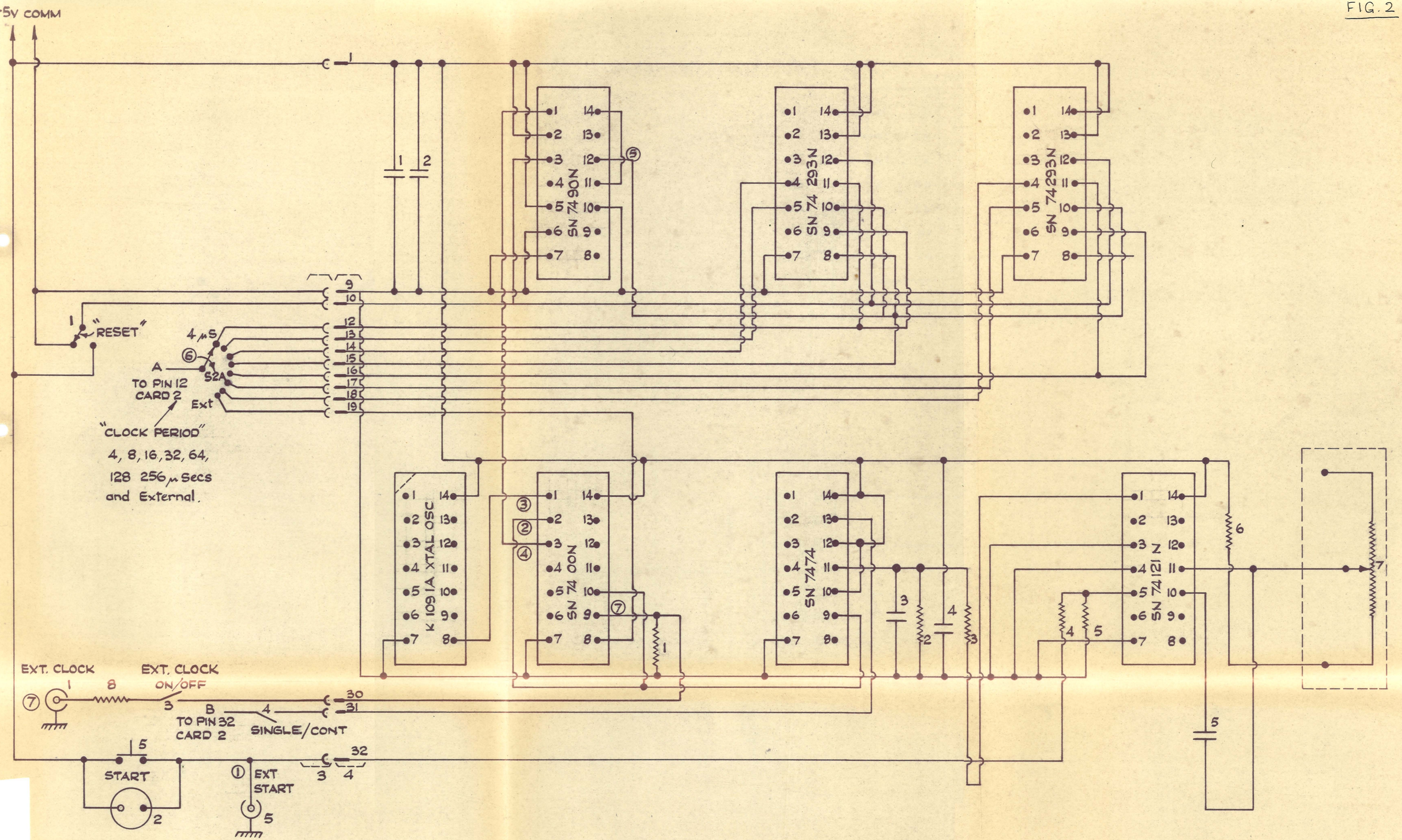
Switches

1	1st Pole of DPCO	RS Components
2	S2A Bank A of Two bank Single Pole Eight Way	RS Components
3	SP On/Off	RS Components
4	SP On/Off	RS Components
5	SP Push Button	Weycom

Connectors

1	BNC Socket fixed	Greenpar
2	2 PIN fixed Size 1	Lemo
3	32 Way Edge Connector	Vero
4	Veroboard band 32 Way	
5	BNC Socket fixed	Greenpar

FIG. 2



AR 239 FIG 2 CARD 1 GATED CLOCK PULSE GENERATOR DRG. No 1323

Key to Components

CARD 2 PROGRAMMABLE-MEMORY ADDRESS AND STOP SIGNAL GENERATOR (Fig 3)

Integrated Circuits

74 Series		Texas Insts

Capacitors

1	0.0022 μF	Ceramic	Erie
2	0.01 μF	Ceramic	Erie
3	0.1 μF		RS Components

Switches

1	See Card 1 Components List	

Connectors

1	32 Way Edge Connector	Vero
2	32 Way Veroboard	

FIG. 3

MSB

MEMORY ADDRESS

LSB

THESE CONNECTIONS GO TO THE MEMORY STACK VIA THE "MANUAL ADDRESS" SWITCH BANK

+5V

CLOCK FROM A CARD 1

COMM

RESET 2

(GANGED TO RESET 1)

COMM

STOP SIGNAL TO B CARD 1

SN 74161N

SN 7420

SN 7400

AR 239 FIG 3 CARD 2 PROGRAMMABLE-MEMORY ADDRESS AND "STOP" SIGNAL GENERATOR DRG Nº1324

Key to Components

CARD 3 PROGRAMMABLE MEMORY STACK (Fig 4)

Integrated Circuits

Memories A,B,C, 512 x 4 bit output - Memory Devices
Program - as per Table 1

Resistors

1	1K5	MR5	Welwyn
2	1K5	MR5	Welwyn
3	1K5	MR5	Welwyn
4	1K5	MR5	Welwyn
5	24K	MR5	Welwyn
6	24K	MR5	Welwyn
7	1K5	MR5	Welwyn
8	1K5	MR5	Welwyn
9	1K5	MR5	Welwyn
10	1K5	MR5	Welwyn
11	1K5	MR5	Welwyn
12	1K5	MR5	Welwyn
13	1K5	MR5	Welwyn
14	1K5	MR5	Welwyn

Capacitors

1	0.01 µF	Ceramic	Erie
2	0.01 µF		RS Components
3	180 pF	Polystyrene	Suflex Type HS
4	560 pF	Polystyrene	Suflex Type HS
5	390 pF	Polystyrene	Suflex Type HS
6	220 pF	Polystyrene	Suflex Type HS
7	220 pF	Polystyrene	Suflex Type HS
8	220 pF	Polystyrene	Suflex Type HS

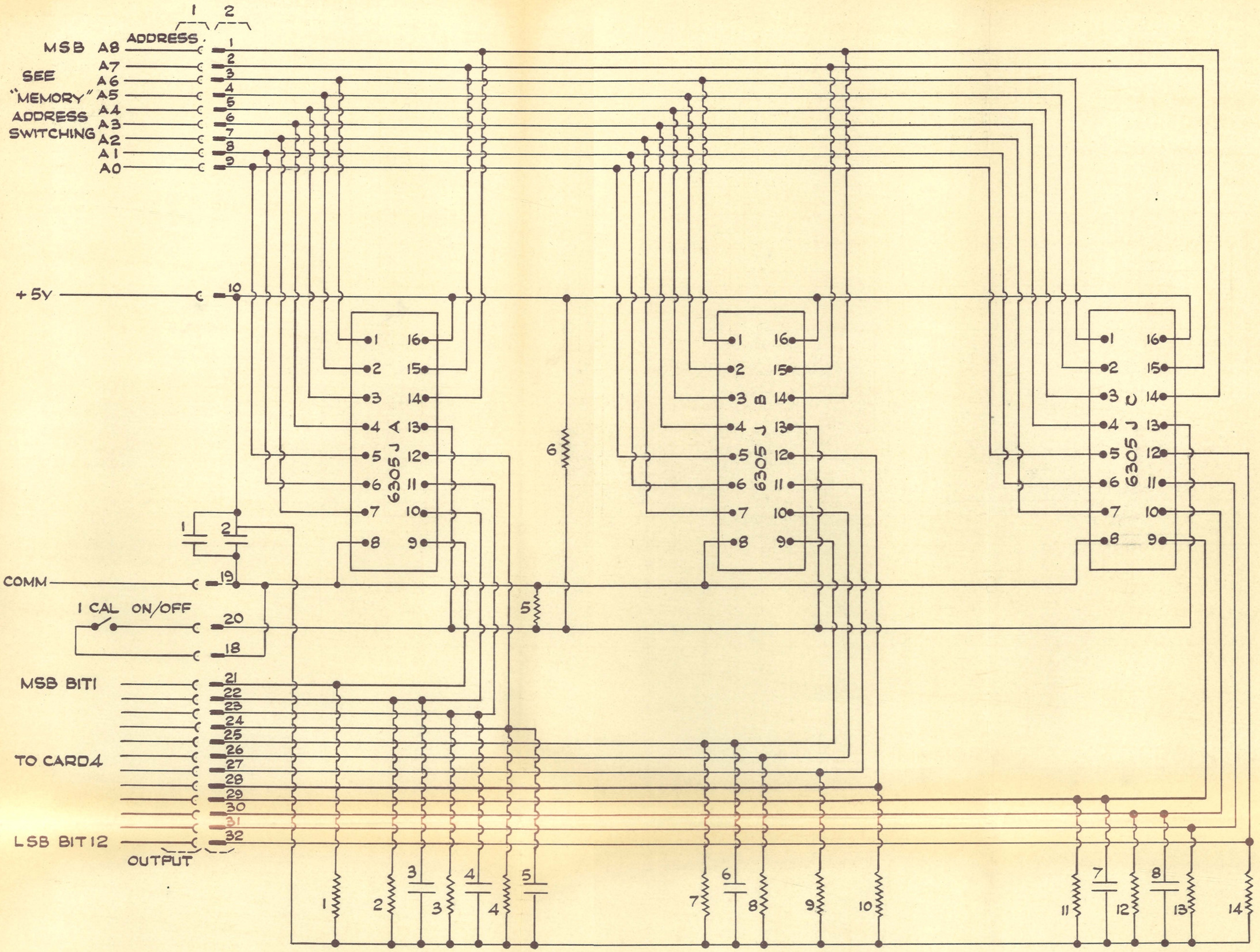
Switches

SP	On/Off

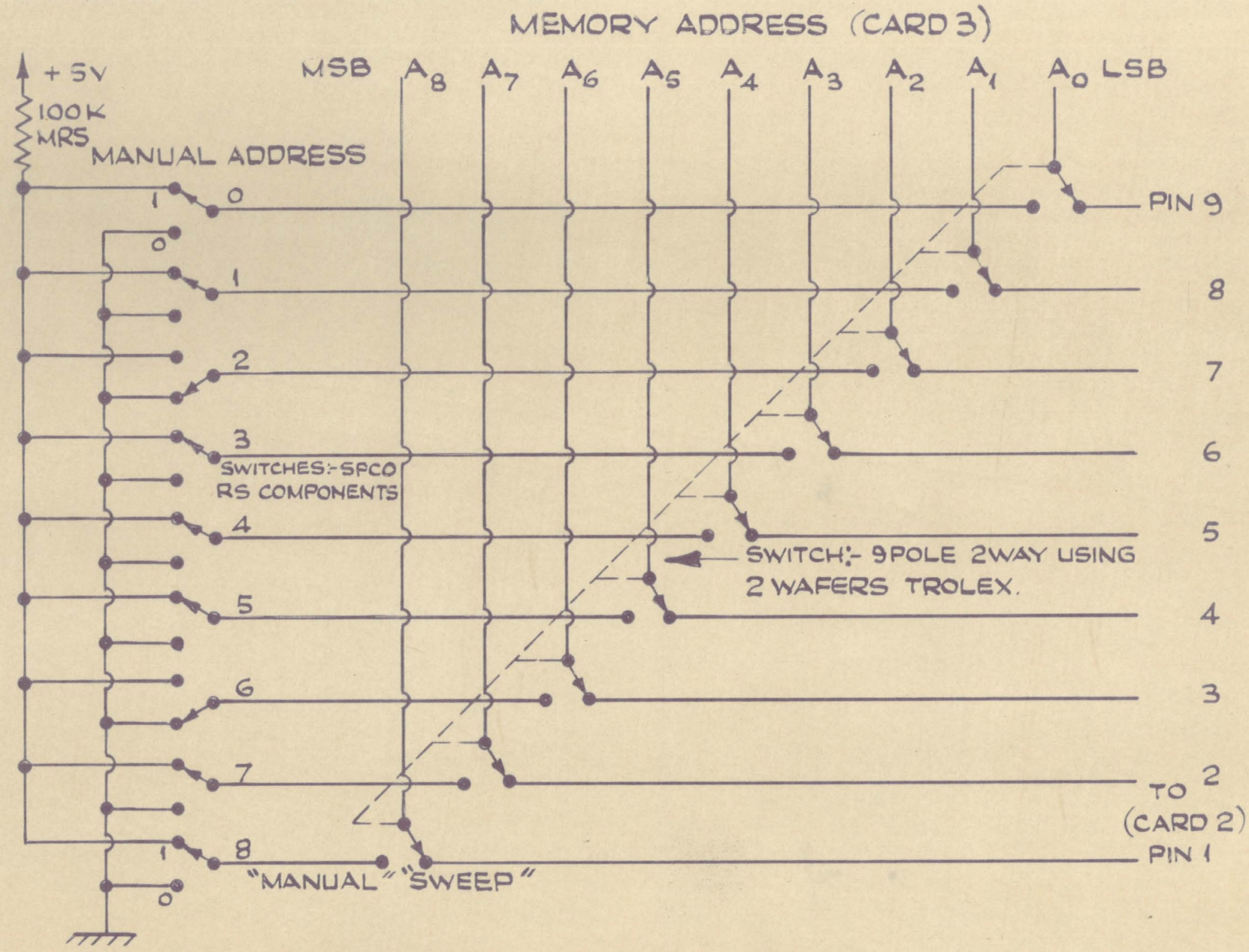
Connectors

1	32 Way Edge Connector	Vero
2	32 Way Veroboard	

FIG. 4



AR 239 FIG.4 CARD 3 PROGRAMMABLE MEMORY STACK. DRG Nº 1325



AR 239 FIG 5 MEMORY ADDRESS SWITCHING ARRANGEMENT. DRG N° 1326

Key to Components

CARD 4 CONNECTIONS TO DIGITAL-ANALOGUE CONVERTER (Fig 6)

D-A Converter	DAC 12QZ BIN	Analogue Devices
Mounting Board	4516	Analogue Devices

Resistors

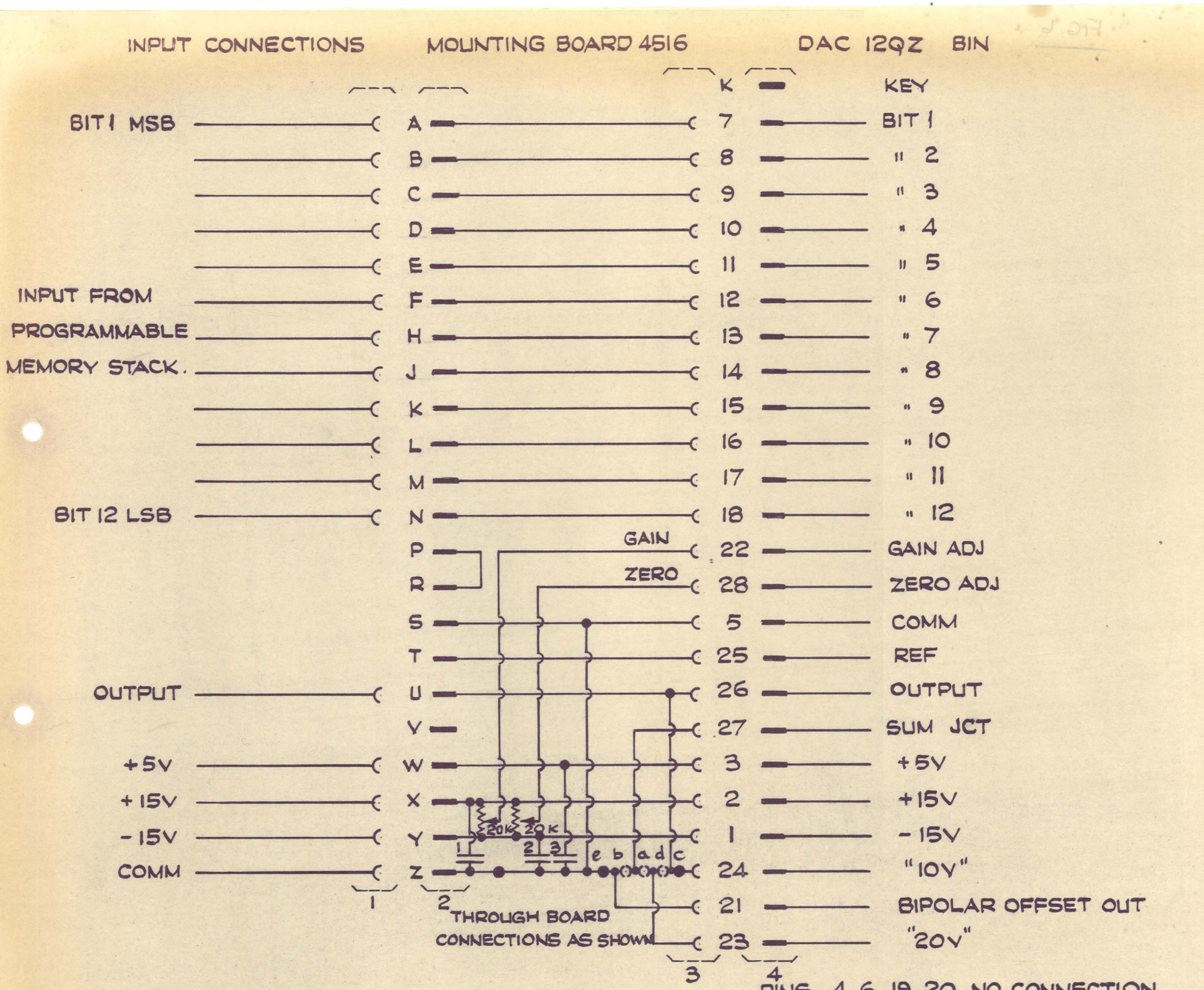
20K Flatpot Potentiometers. Supplied with Mounting Board.

Capacitors

1	0.01 μF	Ceramic	Erie
2	0.01 μF	Ceramic	Erie
3	0.01 μF	Ceramic	Erie

Connectors

1	44 Way Edge Connector Cinch
2	44 Way Mounting Board type 4516
3	0.019 in Socket Matrix
4	Connections from D-A Convertor



AR 239 FIG 6 CARD 4 CONNECTIONS TO DIGITAL-TO-ANALOGUE CONVERTER DRG Nº 1327

Key to Components

CARD 5 INVERTING AMPLIFIER (Fig 7)

Integrated Circuit

SN 72709		Texas Insts

Resistors

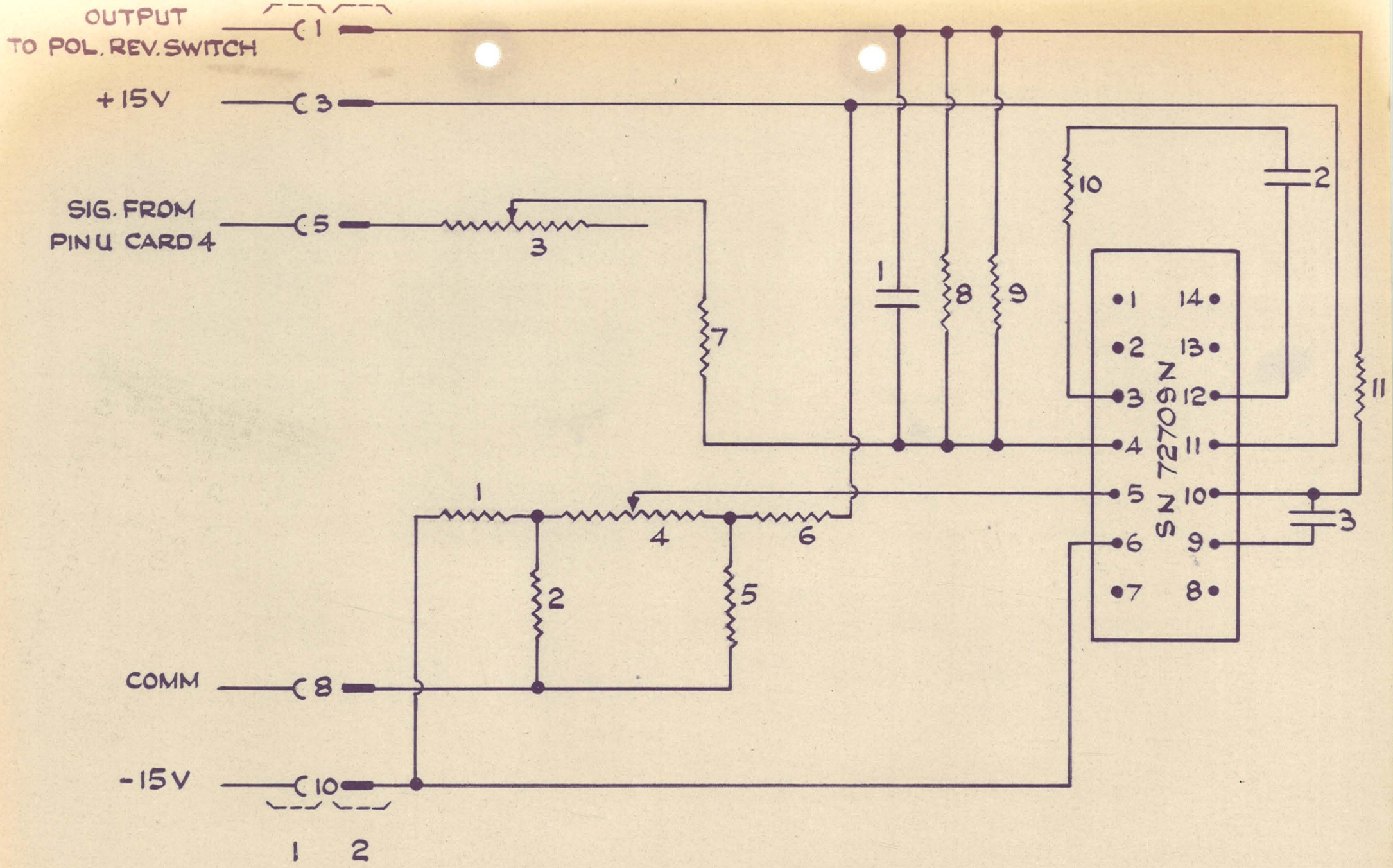
1	10K	Type 4034C	Welwyn
2	22R	Type 4034C	Welwyn
3	1K0	20 Turn Trimpot	Painton
4	1K0	20 Turn Trimpot	Painton
5	22R	Type 4034C	Welwyn
6	10K	Type 4034C	Welwyn
7	47K	Type 4034C	Welwyn
8	47K	Type 4034C	Welwyn
9	2M2	Type 4034C	Welwyn
10	1K5	MR5	Welwyn
11	47R	MR5	Welwyn

Capacitors

1	18 pF	Polystyrene	Suflex
2	4,700 pF	Polystyrene	Suflex
3	220 pF	Polystyrene	Suflex

Connectors

1	16 Way Edge Connector	Vero
2	16 Way Veroboard	



AR 239 FIG 7 CARD 5 INVERTING AMPLIFIER DRG Nº 1328

Key to Components

FILTERING, OUTPUT AND DPM CIRCUITRY (Fig 8)

Resistors

1	150R	4034C	Welwyn
2	5K6	4034C	Welwyn
3	47K	4034C	Welwyn
4	200R	Trimpot	Painton Bourns
5	220R	4034C	Welwyn
6	1K8	4034C	Welwyn
7	47R	4034C	Welwyn
8	240K	MR5	Welwyn
9	4K7	4034C	Welwyn
10	5K	10T Filmpot Type 3501	Bourns (non-inductive)
11	200R	Trimpot	Painton Bourns
12	470K	4034C	Welwyn
13	39K	4034C	Welwyn
14	20K	Trimpot	Painton Bourns
15	4M7	4034C	Welwyn
16	68K	4034C	Welwyn
17	100K	MR5	Welwyn

Capacitors

1	Fitted as required)	
2	4.337 µF ±0.1%)	
3	2.168 µF ±0.1%)	Made up from
4	1.083 µF ±0.1%)	polystyrene (Suflex)
5	0.5408 µF ±0.1%)	and procond
6	0.2696 µF ±0.1%)	(G A Stanley Palmer)
7	0.1340 µF ±0.1%)	capacitors
8	0.06621 µF ±0.1%)	
9	0.01 µF Ceramic	Erie
10	2000 pF from polystyrene (Suflex) and air spaced variable	(100 pF C804) (Jackson Bros)
11	20,000 pF from polystyrene (Suflex) capacitors	
12	2000 pF from polystyrene (Suflex) and air spaced variable	(100 pF C804) (Jackson Bros)
13	20,000 pF from polystyrene capacitors	

Switches

1	Bank B of multi-way switch described on "Card 1"	
2	SP on/off	RS Components
3	DPCO	RS Components
4	SPCO	RS Components
5	SPCO Centre Off	RS Components
6	DPCO Lever Switch	RS Components

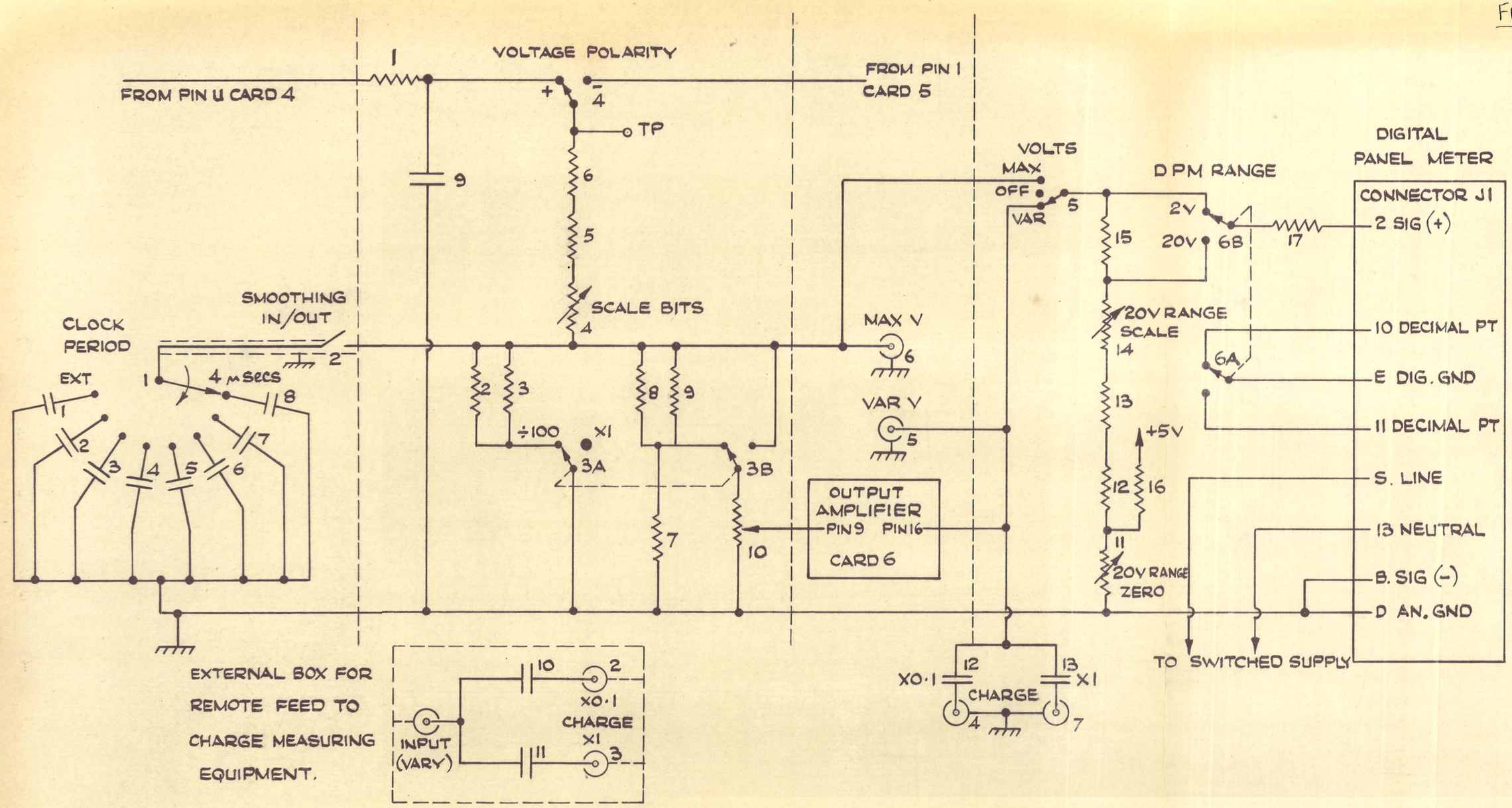
Connectors

1-7	BNC Socket-Fixed	Greenpar
TP	2 mm Socket-Fixed	Radiall

Digital Panel Meter

Analogic Type AN 2553

FIG. 8



AR 239 FIG 8 FILTERING, OUTPUT AND DIGITAL PANEL METER CIRCUIT ARRANGEMENT DRG Nº 1329

Key to Components

CARD 6 OUTPUT AMPLIFIER (Fig 9)

Integrated Circuit

Voltage Follower SN7231ON		Texas Insts

Resistors

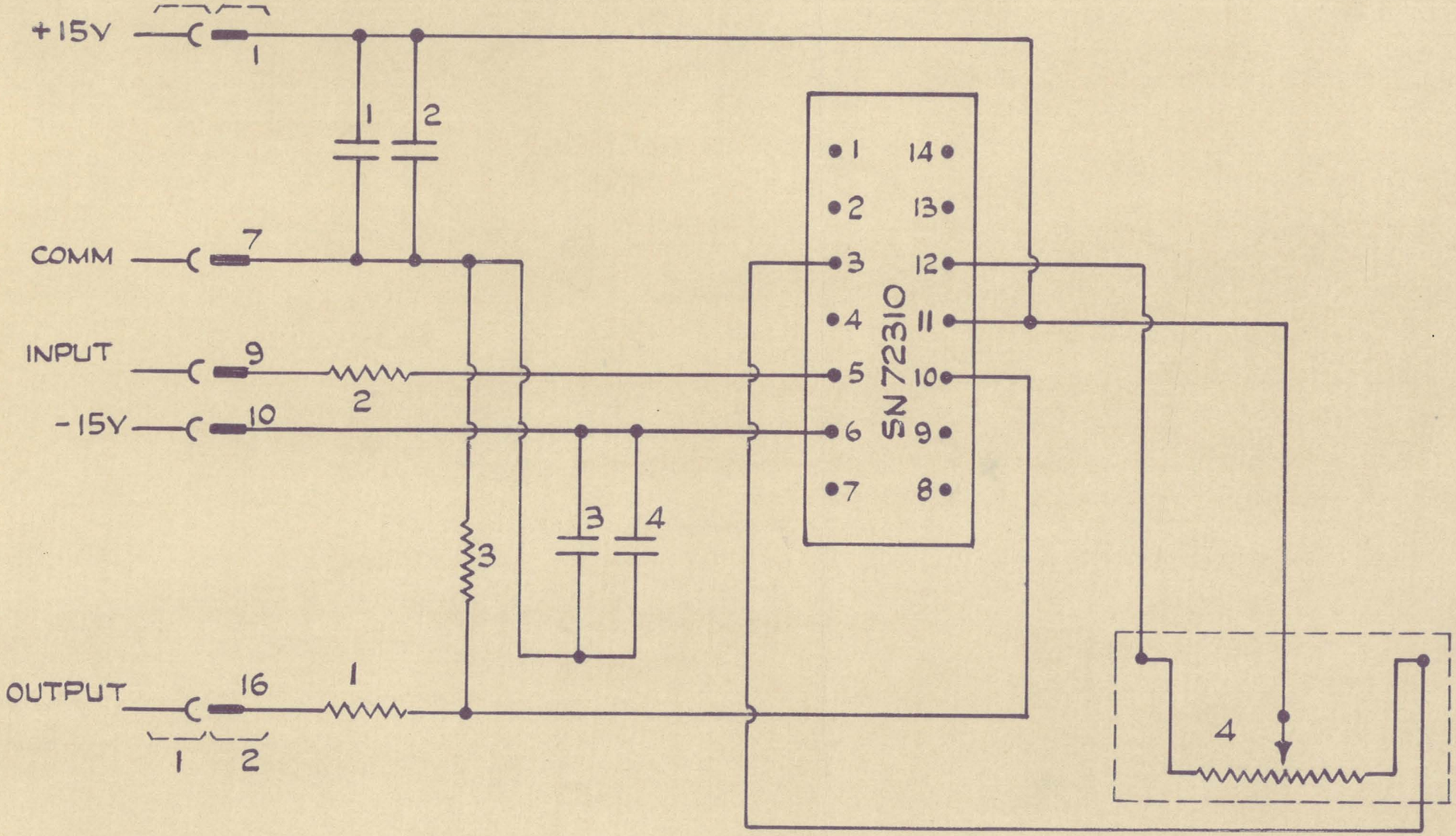
1	47R	MR5	Welwyn
2	10K	MR5	Welwyn
3	10K	MR5	Welwyn
4	1KO	20 Turn Trimpot	RS Components

Capacitors

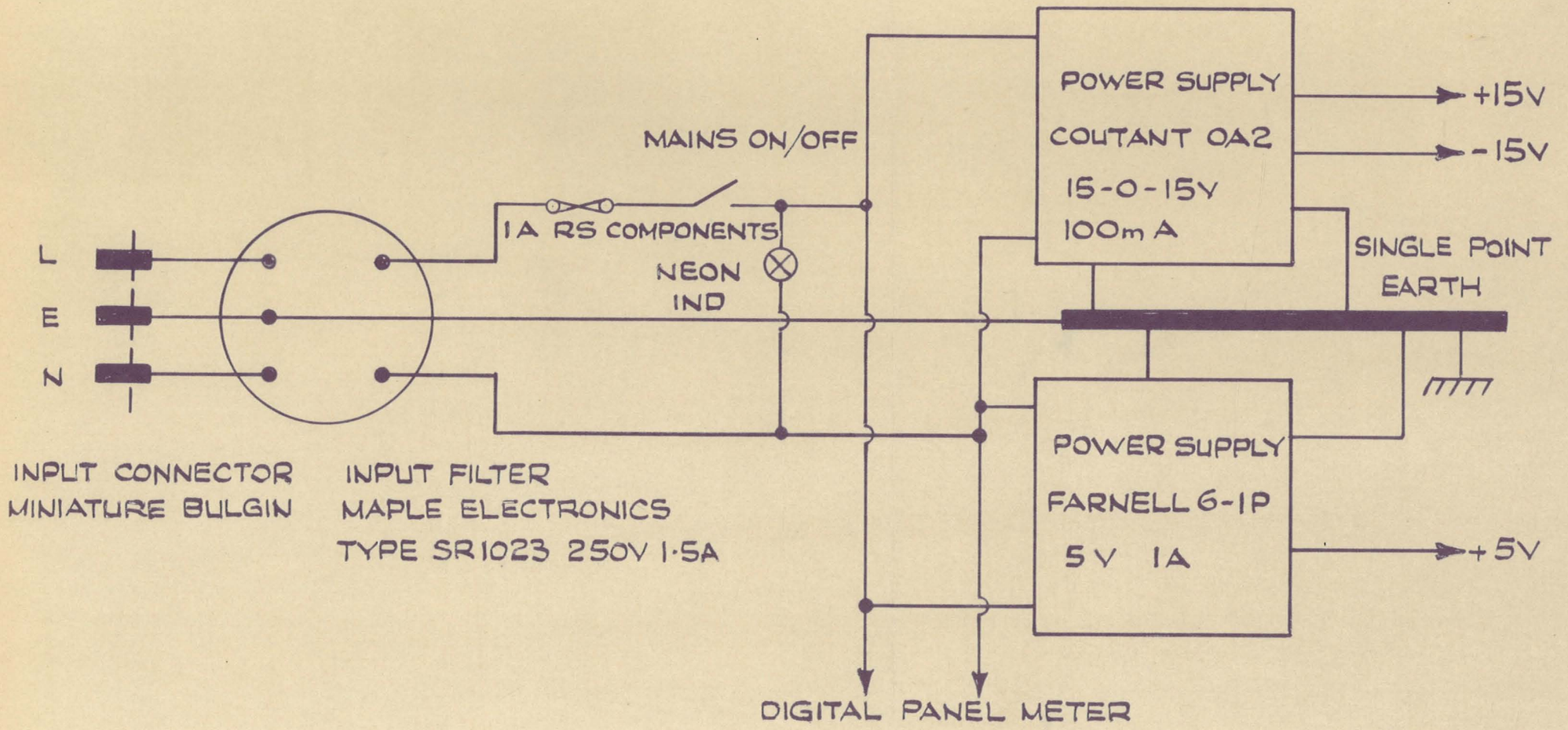
1	0.1 μF	RS Components
2	2,200 pF Ceramic	Erie
3	0.1 μF	RS Components
4	2,200 pF Ceramic	Erie

Connectors

1	16 Way Edge Connector	Vero
2	16 Way to 22 Strip Veroboard	



AR 239 FIG 9 CARD 6 OUTPUT AMPLIFIER DRG Nº 1330



AR 239 FIG 10 POWER SUPPLY ARRANGEMENT DRG Nº 1331

FIG. 11

START

① 0·5-22·0 m sec — SIGNAL RISES AT A TIME EQUAL TO THE DURATION OF "IGNITION DELAY" AFTER THE OPERATION OF THE "START" SWITCH

②

SCALE:- 1cm = 0·1 μ sec

③ 0·2 μ sec

④

④ (OPPOSITE) PHASE IN ③

⑤ 0·7 to 0·9 μ sec — 2·0 μ sec.

SCALE REDUCED BY A FACTOR OF TEN (1cm = 1·0 μ sec)

⑤ 2·0 μ sec

⑥ 8·0 μ sec

⑦

⑧ PIN 14 OF SN74161N — 0·5-22·0 m sec | 0·7-0·9 mSec | 3 μ sec

⑨

⑩

⑯ t_1 PIN 14 OF 3RD SN74161N — t_2

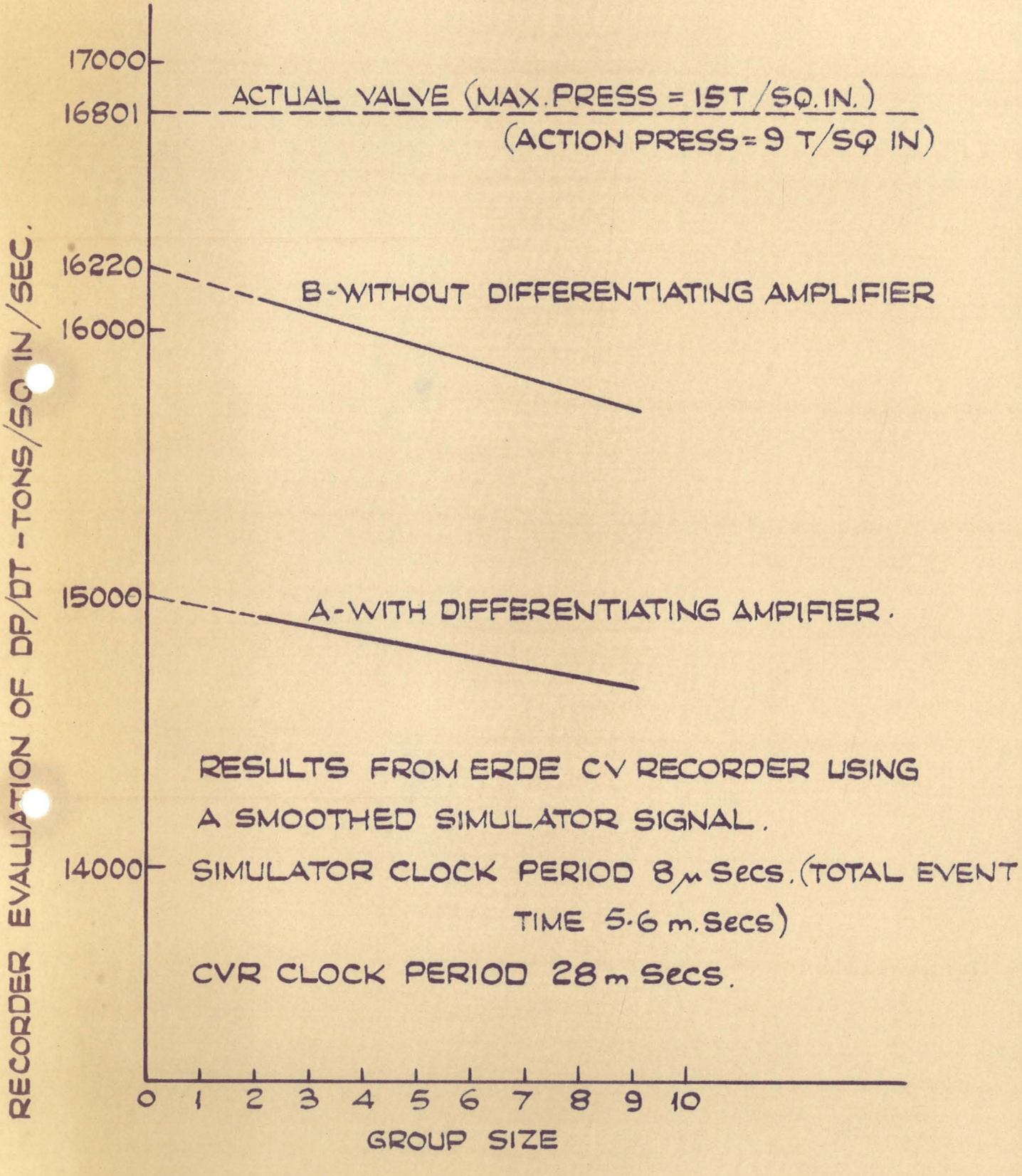
t_1 = IGNITION DELAY(AS SET) + (0·7-0·9) μ Secs + $\frac{\text{CLOCK PERIOD}}{2}$ - 1·0 μ sec

t_2 = CLOCK PERIOD × 255 AND ALL OUTPUTS ARE HIGH AT A TIME = CLOCK PERIOD × 510 AFTER THE END OF t_1

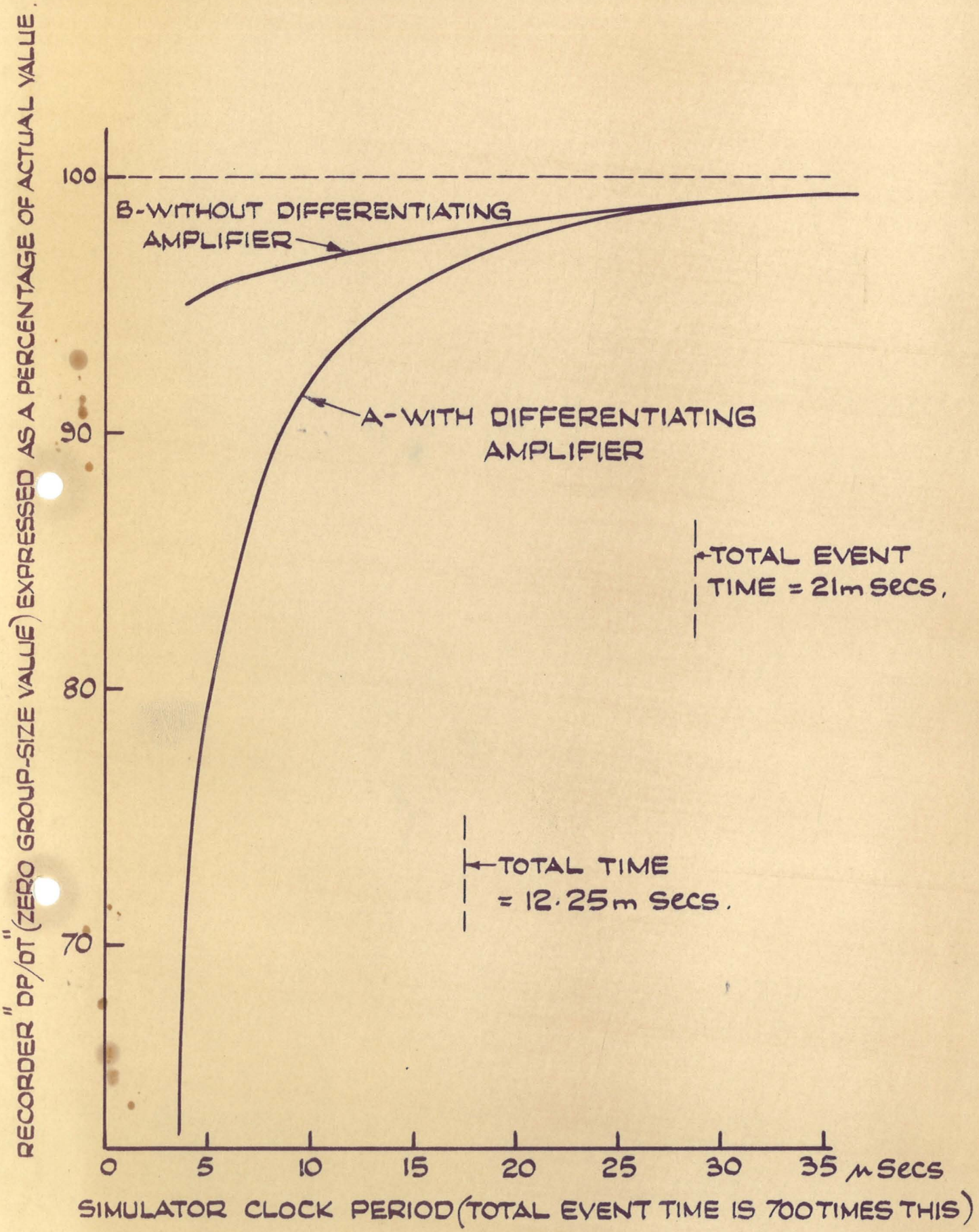
	CHANGE →									
1ST SN74161N PIN 14	0	1	1	0	0	1	1	0	1	0
" " " 13	0	0	0	1	1	1	1	0	1	0
12	0	0	0	0	0	0	0	0	0	1
11	0		0	0	0	0	0	0	0	0
2ND SN74161N PIN 14	0		0	0	0	0	0	0	0	0
	0		0	0	0	0	0	0	0	0
etc	0		0	0	0	0	0	0	0	0
	0		0	0	0	0	0	0	0	0
3RD SN74161N PIN 14	0		0	0	0	0	0	0	0	0

ALL LEVELS STANDARD TTL

AR 239 FIG 11 DIGITAL TIMING WAVEFORMS DRG Nº 1331



AR 239 Fig 12 EFFECT OF GROUP SIZE ON DP/DT EVALUATION. DRG. Nº 1350



AR 239 Fig 13 ERROR CURVES DETERMINED USING THE SIMULATOR SIGNAL DRG Nº 1351

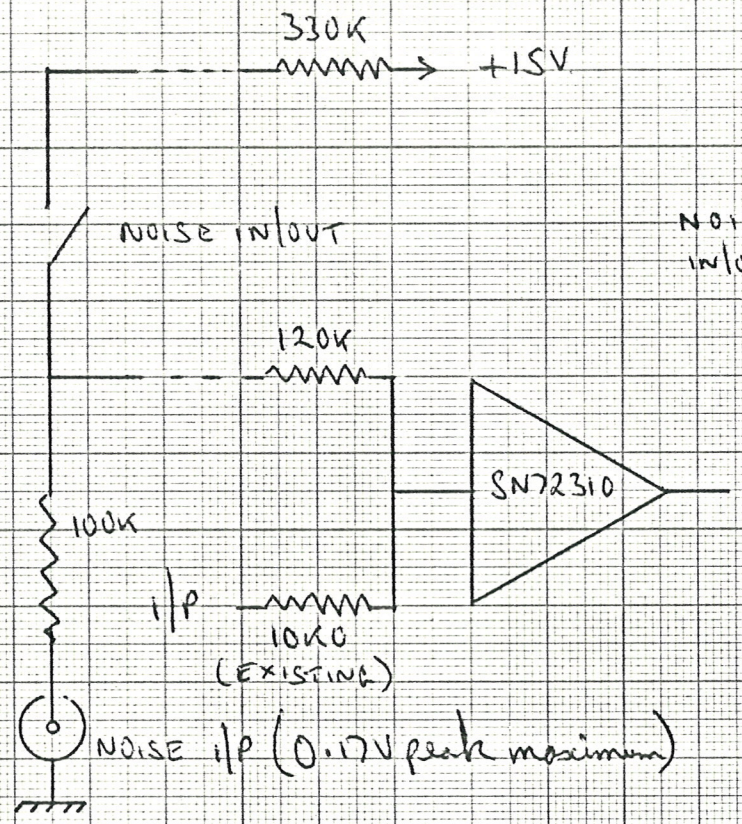
APPARATUS NOTE

CLOSED VESSEL SIGNAL SIMULATOR- AMENDMENT TO ALLOW NOISE ADDITION

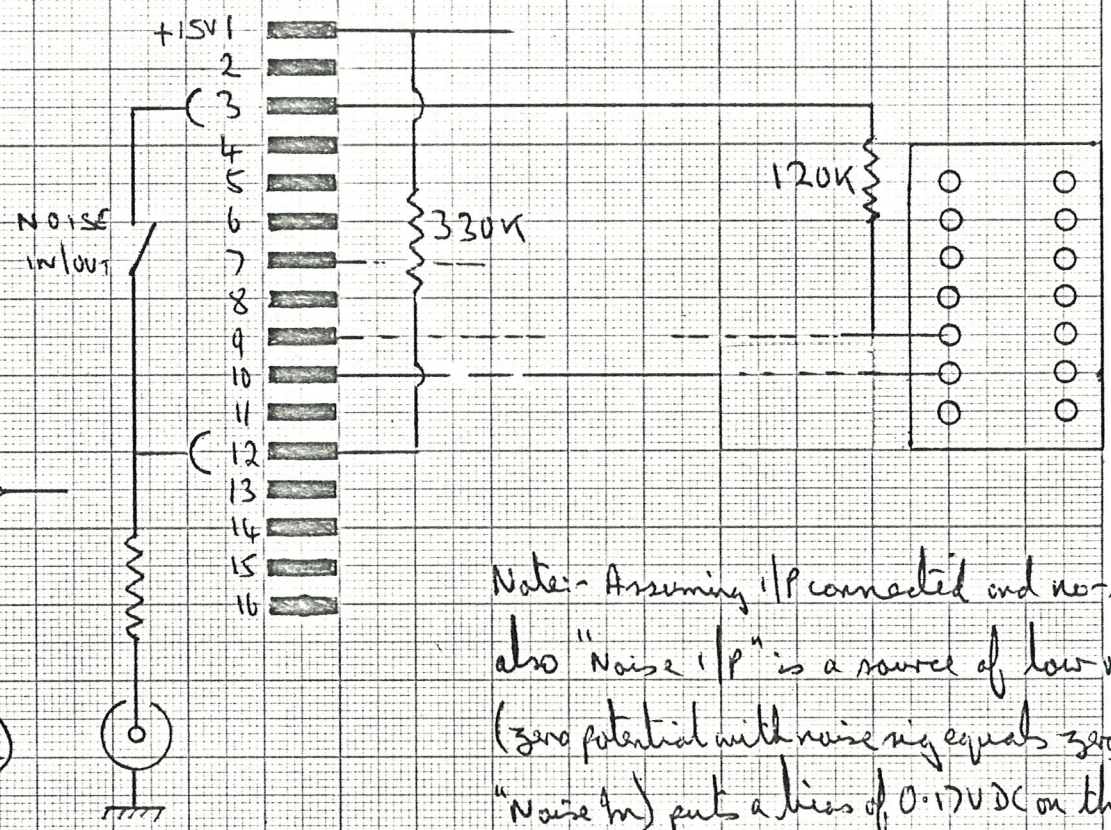
NOVEMBER 1976

D. ELDRIDGE
INSTRUMENTATION
E.R.D.E.

DRG Nº 110N



NEW BASIC CIRCUIT



ADDITIONAL WIRING DIAGRAM

Note:- Assuming I/P connected and no signal also "Noise I/P" is a source of low resistance (zero potential with noise sig equals zero) then "Noise In" puts a bias of 0·17V DC on the 310 input.

AN110 CLOSED VESSEL SIGNAL SIMULATOR - AMENDMENT TO ALLOW NOISE ADDITION